

Atty. Docket No. PIA31205/ANS/US
Application No.: 10/764,905

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Remarks

Applicant and his representatives wish to thank Examiner Sullivan for the thorough examination of the present application and the detailed explanations in the Office Action dated June 14, 2007, including . The following remarks shall further summarize and expand upon topics discussed.

The present invention relates to a method for forming a metal line. The method (as set forth in Claim 1) generally comprises:

- a) stacking a lower insulating layer, a lower metal line and an upper insulating layer;
- b) patterning a first photosensitive film on the upper insulating layer;
- c) using the patterned first photosensitive film as a mask, etching the upper insulating layer until at least a portion of the lower metal line is exposed;
- d) filling an etched portion of the upper insulating layer with a nitride film;
- e) patterning a second photosensitive film over the lower metal line and the nitride film;
- f) using the second photosensitive film as a mask, etching the lower metal line until the lower insulating layer is exposed to form a lower metal line pattern;
- g) depositing an IMD (Inter Metal Dielectric) layer on the lower metal line pattern and the nitride film, thereby forming an air gap in the IMD layer between lines in the lower metal line pattern;
- h) planarizing the IMD layer to expose the nitride film;
- i) removing the nitride film, thereby forming a contact hole in the IMD layer exposing an upper surface of the lower metal line;
- j) filling the contact hole with a conductive material; and

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k) depositing an upper metal line over the conductive material.

The present method forms an air gap in an intermetal dielectric (IMD) layer between lines in a lower metal line pattern. The air gap is formed as a result of depositing the IMD layer on the lower metal line pattern and the nitride film [step g above], which is formed at least in part on the lower metal line pattern (i.e., by filling an etched portion of an upper insulating layer exposing the lower metal line with a nitride film [step d above], then etching the lower metal line until the lower insulating layer is exposed to form a lower metal line pattern [step f above]). Then, after forming the air gap in the IMD layer, the nitride film is removed, thereby forming a contact hole in the IMD layer exposing an upper surface of the lower metal line.

None of the references cited against the present claims (Furukawa et al, U.S. Pat. No. 6,221,704 [hereinafter "Furukawa"], Wang, U.S. Pat. No. 6,159,840 [hereinafter "Wang"], Grill et al., U.S. Pat. No. 6,737,725 [hereinafter "Grill"], Gardner et al., U.S. Pat. No. 5,869,379 [hereinafter "Gardner"] and Yasushi, JP 2-047840 [hereinafter "Yasushi"]) disclose or suggest etching a lower metal line using *a second photosensitive film* as a mask until the lower insulating layer is exposed to form a lower metal line pattern, or depositing an IMD layer on the lower metal line pattern and a nitride film thereon, *thereby forming an air gap* in the IMD layer between lines in the lower metal line pattern (see Claim 1). Consequently, no possible combination of the cited references can disclose or suggest all of the limitations of Claim 1. As a result, the present claims are patentable over the cited references.

The Rejection of Claims 1-5 (and 7?) under 35 U.S.C. § 103(a)

The rejection of Claims 1-5 (and, apparently, 7) under 35 U.S.C. § 103(a) as being unpatentable over Furukawa and Wang, in view of Grill and Gardner is respectfully traversed.

Furukawa discloses a process for fabricating a short channel field effect transistor with a highly conductive gate (Title). As noted in the final Office Action, Furukawa teaches forming second conductive layer 27 on the first conductive-forming layer 4 (col. 7, ll. 54-56, and FIG. 5). Suitable conductive materials 27 include tungsten, tungsten silicide, titanium silicide, cobalt

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silicide and titanium nitride (col. 7, ll. 57-59). Only one of the suitable materials is a metal (tungsten); the remaining examples are metal compounds. As will be explained later, under the processing conditions disclosed by Furukawa, even that one example of a metal layer is converted to a metal compound prior to deposition of the insulator layer in which contact holes are formed.

Significantly, as the conductive forming layer 4, Furukawa discloses only doped polysilicon or intrinsic polysilicon with doping ions implanted into it (col. 3, ll. 42-59, and FIGS. 1-3). To one of ordinary skill in the art, this identifies the stacked structures 3/4/7 and 3/4/27/28 of Furukawa as a *polysilicon* line or polycide layer, rather than a metal line or metal layer (see Wolf, *Microchip Manufacturing*, Lattice Press, Sunset Beach, California [2004], pp. 54-55 and 60-67; and Wolf et al., *Silicon Processing for the VLSI Era*, vol. 1, Lattice Press, Sunset Beach, California [2000], pp. 723-724, submitted herewith). This distinction is important, in that one of ordinary skill in the art would not necessarily apply a process or technique used in forming a poly layer to a method of forming a metal layer, or vice versa. In fact, Furukawa distinguishes metal lines M1 from the gate (poly) layer structures 3/4/7 and 3/4/27/28 (see, e.g., col. 7, ll. 47-49 and col. 9, ll. 1-7).

Thus, Furukawa does not disclose stacking a lower insulating layer, *a lower metal line* and an upper insulating layer, as recited in Claim 1.

Furthermore, Furukawa does not show *adjacent* stacked gate structures 3/4/27/28, presumably because they are too far apart to be shown on the scale of the drawings in Furukawa. Thus, one of ordinary skill in the art would not necessarily conclude that forming an air gap between adjacent stacked gate structures is even possible, much less desirable. However, assuming for the sake of argument that it might be possible, one of ordinary skill in the art would recognize that altering the process of Furukawa to require forming an air gap between adjacent stacked gate structures 3/4/27/28 could have catastrophic consequences. The contacts CA (and thus the corresponding contact holes) in FIGS. 4 and 8 of Furukawa would have to be formed in the same space (i.e., between adjacent stacked gate structures). If the contact hole overlaps the air gap, it would be challenging to reliably form uniform contacts CA. For example, the opening

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of the contact hole could be smaller than the combined width of the contact hole and the air gap, in which case the opening to the contact hole could close before the combined contact hole and air gap was filled with contact-forming material (see Wolf et al., *Silicon Processing for the VLSI Era*, vol. 1, Lattice Press, Sunset Beach, California [2000], pp. 210-211 and 217, submitted herewith, which respectively show phenomena resulting in voids when a metal deposited into a trench or contact hole by CVD [Fig. 6-47] or sputtering [Fig. 6-53] closes or begins to close at the opening before the contact hole is completely filled). A relatively small contact hole opening would be expected to result in voids (see Wolf et al., p. 211), which would be expected to significantly affect the uniformity of contact resistance, and thus, have an adverse impact on yield. Thus, one of ordinary skill in the art would not be at all motivated to modify the process or structure of Furukawa to include an air gap between conductive structures, nor would one of ordinary skill in the art be at all motivated to substitute the stacked gate structures 3/4/27/28 of Furukawa for a stacked lower insulating layer, lower metal line and upper insulating layer typical of metallization layers.

As a result, the disclosure of Furukawa is deficient with regard to (and is arguably essentially irrelevant to) the presently claimed method. (It is noted for the record that Furukawa heats the wafer to drive dopant from a dopant source into the polysilicon gate and S/D extension regions; see col. 8, ll. 40-47. At typical dopant drive-in times and temperatures [see Wolf, p. 62], any metal 27 deposited on polysilicon gate layer 4 in Furukawa may be expected to form silicide [see Wolf, p. 63], which raises a further question about whether Furukawa discloses a stacked lower insulating layer, lower *metal* line and upper insulating layer, at least where one would remove the nitride film to form a contact hole exposing an upper surface of the lower metal line.)

Wang discloses forming a metal layer 202 on the substrate 200 as the bottom layered conductive line of the metal interconnect (col. 2, ll. 49-51 and FIGS. 1 and 2A). A dielectric layer 204 is further formed covering the metal layer 202 and the substrate 200, and thereafter, a stop layer 206 is formed on the dielectric layer 204 (for example, a silicon nitride layer; see col. 2, ll. 51-57 of Wang). A dielectric layer 208 (for example, an oxide layer) is further formed on the stop layer 206 (col. 2, ll. 57-59 of Wang).

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Wang then teaches defining the dielectric layer 208, the stop layer 206 and the dielectric layer 204 using a photoresist layer 210, followed by removing the portions of the dielectric layer 208, the stop layer 206 and the dielectric layer 204 not covered by the photoresist layer 210 to form a via opening 212a and an opening 212b where the air-gap is to be formed (col. 2, ll. 60-67 and FIGS. 1 and 2B). Wang then forms a dielectric material 214 (such as a PECVD oxide layer) on the dielectric layer 208 (col. 3, ll. 7-9 and FIG. 2C). The recipe for forming the dielectric material 214 is adjusted during the deposition process to result in a dielectric material 214 with a slightly inferior step coverage property. The dielectric material 214 thus directly covers the dielectric layer 208, sealing the opening 212b (as in FIG. 2B) to form an air gap 213, but not completely filling the opening 212b (col. 3, ll. 10-15 of Wang). Furthermore, the dielectric material 214 also covers the via opening 212a, resulting in a part of the dielectric material 214 partially filling the via opening 212a. The height of the dielectric material 214 in the via opening 212a and the opening 212b is controlled to be above the stop layer 206, which is favorable in forming the air-gap 213 and manufacturing the via plug (col. 3, ll. 15-22 of Wang).

Wang then forms a photoresist layer 216 on the dielectric material 214, and forms a trench 218 in the dielectric material 214 and the dielectric layer 208 (see FIGS. 2D-2E and col. 3, ll. 23-27 of Wang). The trench 218 is formed by anisotropic etching of the dielectrics 214 and 208 using the stop layer 206 as an etch-stop. The dielectric material 214 and the dielectric layer 208 are completely removed in the via opening 212a to expose the metal layer 202. On the other hand, the dielectric material 214 above the air-gap 213, protected by the photoresist layer 216, remains (col. 3, ll. 27-37 and FIG. 2E of Wang).

Thus, like Furukawa, Wang fails to etch *the lower metal line* using the second photosensitive film as a mask. Thus, it is irrelevant whether Wang etches dielectric materials or exposes the lower metal layer by etching using the second photosensitive film as a mask. Wang fails to cure this deficiency of Furukawa with regard to the present Claim 1.

Furthermore, like Furukawa, Wang fails to deposit an IMD layer on the lower metal line pattern and the nitride film, thereby forming an air gap in the IMD layer between lines in the lower metal line pattern. The air gap 213 in Wang is formed in dielectric layers 204 and 208

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(FIG. 2B), or between dielectric layer 214 and substrate 200 (FIG. 2C) by deposition of dielectric layer 214. (Stop layer 206 of Wang corresponds to the present nitride layer.) Thus, to the extent that depositing dielectric layer 214 forms air gap 213, the air gap 213 is not in dielectric layer 214, but in one or more other dielectric layers, or between dielectric layer 214 and another structure. Thus, Wang fails to cure this second deficiency of Furukawa with regard to the present Claim 1.

According to Furukawa, the second insulating layer 5, the second conductive layer 27 and the conductive material 4 are etched using the third insulating material 28 as a mask, to form a part of the gate stack (see col. 8, ll. 24-36). However, according to Wang, a photoresist layer 216 is used as a mask to define the dielectric material 214 and the dielectric layer 208 (see col. 3, ll. 23-39). Thus, Furukawa discloses etching a lower conductor until the lower insulating layer is exposed, but not using a photosensitive film as a mask to do so. By contrast, Wang discloses using a second photoresist layer as an etch mask, but to pattern a dielectric material. As a result, it is considered improper to use the combination of Furukawa and Wang as a basis for finding the step of etching the lower metal line using the second photosensitive film as a mask. It is believed that etching conditions are generally determined according to the material(s) being etched and the material used as a mask. Consequently, processes for etching a conductor may not be interchangeable with processes for etching a dielectric, and processes for etching using a photoresist layer may not be interchangeable with processes for etching using a dielectric material as a hard mask.

(It is further noted that Wang, like Furukawa, fails to teach, disclose or suggest *planarizing* dielectric layer 214 to expose stop layer 206, thereby failing to teach or suggest the presently claimed step of planarizing the IMD layer to expose the nitride film, or filling an etched portion of the upper insulating layer with a nitride film.)

Grill and Gardner fail to cure the deficiencies of Furukawa and Wang.

Grill discloses a method for forming a multilayer interconnect structure that includes interconnected conductive wiring and vias spaced apart by a combination of solid or gaseous

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dielectrics (Abstract, ll. 1-4). The method includes the steps of: (a) forming a first planar via plus line level pair embedded in a dielectric matrix formed from one or more solid dielectrics, wherein at least one of said solid dielectrics is at least partially sacrificial; (b) etching back sacrificial portions of the sacrificial dielectrics to leave cavities extending into and through the via level, while leaving at least some of the original via level dielectric as a permanent dielectric under the lines; (c) partially filling or overfilling the cavities with a place-holder material; (d) planarizing the structure by removing overfill of the place-holder material; (e) repeating steps (a)-(d) as necessary; (f) forming a dielectric bridge layer over the planar structure; and (g) forming air gaps by at least partially extracting the place-holder material (Abstract, ll. 4-end).

Like Furukawa and Wang, Grill fails to etch the lower metal line using a photosensitive film as a mask. In fact, Grill explicitly teaches patterning dielectric layers 110-140 and overfilling the cavities in dielectric layers 110-140 with diffusion barrier material 170 and conductive material 180, then removing the overfill by chemical mechanical polishing (CMP; see col. 5, ll. 22-37 and FIGS. 1C-1E). Thus, Grill does not cure the first deficiency of Furukawa and Wang with regard to the present Claim 1.

Grill teaches that the structure of FIG. 1G (containing wiring structures 185) is overfilled with a sacrificial place-holder (SPH) material 220 to form the structure of FIG. 1H (col. 6, ll. 20-45). It is preferred that the SPH be a material that "gap fills" in a way *that does not leave cavities* that will be opened when the SPH is planarized (col. 6, ll. 50-53). After forming the desired number of wiring and via levels (i.e., patterned conductors embedded in a dielectric matrix comprising permanent dielectric materials and SPH materials; see col. 7, ll. 1-5 and FIG. 1L), dielectric bridge layer 250 is formed and patterned with small openings (holes or perforations) 260 to produce the structure of FIG. 1M (see col. 7, ll. 5-7 of Grill). SPH material 220' and 220 in FIG. 1M is then extracted to form the structure of FIG. 1N, with air gaps 270 (col. 7, ll. 35-36). Thus, like Furukawa and Wang, Grill fails to disclose depositing an IMD layer on the lower metal line pattern and the nitride film, thereby forming an air gap in the IMD layer between lines in the lower metal line pattern. As a result, Grill fails to cure the second deficiency of Furukawa and Wang with regard to the method recited in Claim 1.

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(Also like Furukawa and Wang, Grill further fails to disclose planarizing an IMD layer to expose the nitride film. Again, Grill is arguably essentially irrelevant to the presently claimed method.)

Like Furukawa, Gardner discloses a process for forming a transistor (Abstract, l. 1). As is discussed in *Wolf* and *Wolf et al.*, formation of a transistor occurs at or below the polysilicon level in a CMOS integrated circuit. As a result, the teachings of Gardner may not have much (if any) bearing on the present method, which begins by stacking a lower insulating layer, a lower *metal* line and an upper insulating layer.

Gardner teaches that an isotropic etch may be performed on exposed lateral surfaces of *polysilicon gate conductors 18* such that the gate conductors are selectively narrowed to a pre-determined lateral thickness (see col. 5, ll. 46-49 and FIG. 6). While masking structures 20 are preferably composed of nitride, they may comprise oxide, silicon oxynitride, or a metal. Thus, depending on whether masking structures 20 are nitride or a metal, Gardner discloses either filling an etched portion of the upper insulating layer with a nitride film or stacking a lower insulating layer, a lower metal line and an upper insulating layer. It appears that Gardner cannot disclose both.

Like Furukawa, Wang and Grill, Gardner fails to etch a lower metal line using a second photosensitive film as a mask. Like Furukawa, Gardner teaches removing select portions of polysilicon layer 14 and masking layer 16 to form a gate conductor 18 with overlying masking structure 20 using optical lithography and a dry plasma etch technique (see col. 5, ll. 31-38 and FIG. 4). Thereafter, Gardner discloses that an isotropic etch may be performed on exposed lateral surfaces of polysilicon gate conductors 18 such that the gate conductors are selectively narrowed to a pre-determined lateral thickness (col. 5, ll. 46-49 and FIG. 6). The isotropic etch technique preferably involves using a wet etchant that exhibits high selectivity for polysilicon such that gate conductors 18 may be etched without significant etching of the overlying masking structures 20 (col. 5, ll. 49-53), thereby indicating to one of ordinary skill in the art that masking structure 20 is used as the mask for the isotropic etch of polysilicon gate conductors 18. Thus, assuming for the sake of argument that polysilicon gate conductors 18 correspond to the

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presently claimed lower metal line, Gardner does not etch the lower "metal" line using a second photosensitive film as a mask. As a result, Gardner does not cure the first deficiency of Furukawa, Wang and Grill with regard to the present Claim 1.

After further processing, Gardner teaches that an interlevel dielectric 38 may be CVD deposited from, e.g., a TEOS source across exposed surfaces of the semiconductor topography (col. 6, l. 66-col. 7, l. 1 and FIG. 11). The presence of masking structures 20 above gate conductors 18 may prevent the accumulation of dielectric material upon the sidewall surfaces of gate conductors 18. As a result, air gaps 40 may be formed laterally *adjacent to gate conductors 18* underneath the masking structures 20 (col. 7, ll. 1-6; emphasis added). Thus, Gardner deposits a dielectric material such that air gaps are formed *between* the dielectric material and polysilicon gate conductors 18, rather than *in* the dielectric material, between lines in the lower metal line pattern.

Thus, like Furukawa, Wang and Grill, Gardner fails to disclose depositing an IMD layer on a lower metal line pattern and the nitride film (recall that masking structures 20 can be *either* metal *or* a nitride, not both), thereby forming an air gap in the IMD layer between lines in the lower metal line pattern. As a result, Gardner fails to cure the second deficiency of Furukawa, Wang and Grill with regard to the method recited in Claim 1.

Furthermore, Gardner appears to be silent with regard to removing masking structures 20, forming structures that replace masking structures 20, or forming structures that are over such masking structures 20 or replacement structures. Therefore, Gardner fails to disclose removing a nitride film to thereby form a contact hole in an IMD layer and expose an upper surface of the lower metal line (or any step subsequent thereto), as recited in the present Claim 1.

As a result, it is believed that no possible combination of the cited references discloses or suggests removing a nitride film to thereby form a contact hole in an IMD layer and expose an upper surface of the lower metal line, as recited in amended Claim 1 above. Consequently, this ground of rejection is unsustainable, and should be withdrawn.

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The Rejection of Claim 8 under 35 U.S.C. § 103(a)

The rejection of Claim 8 under 35 U.S.C. § 103(a) is respectfully traversed.

Claim 8 depends from Claim 1, and thus contains all of the limitations of Claim 1. As mentioned above, the combination of Furukawa, Wang, Grill and Gardner is deficient with regard to (1) etching a lower metal line using *a second photosensitive film* as a mask until the lower insulating layer is exposed to form a lower metal line pattern, and (2) depositing an IMD layer on the lower metal line pattern and a nitride film thereon, *thereby forming an air gap* in the IMD layer between lines in the lower metal line pattern, as recited in Claim 1. Yasushi fails to cure these deficiencies.

Although Yasushi discloses removing a nitride layer by wet etching, Yasushi appears to be silent with regard to etching a lower metal line using a second photosensitive film as a mask until the lower insulating layer is exposed to form a lower metal line pattern as claimed in Claim 1, and depositing an IMD layer on the lower metal line pattern and a nitride film thereon, thereby forming an air gap in the IMD layer between lines in the lower metal line pattern, as recited in Claim 1. Thus, for essentially the same reasons as set forth above for Claim 1, Claim 8 is patentable over the combination of Furukawa, Wang, Grill, Gardner and Yasushi. Accordingly, this ground of rejection is unsustainable, and should be withdrawn.

Conclusions

In view of the above remarks, all bases for objection and rejection are overcome, and the application is in condition for allowance. Early notice to that effect is earnestly requested.

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If it is deemed helpful or beneficial to the efficient prosecution of the present application, the Examiner is invited to contact Applicant's undersigned representative by telephone.

Respectfully submitted,



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**SILICON PROCESSING
FOR
THE VLSI ERA**

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**STANLEY WOLF Ph.D.
RICHARD N. TAUBER Ph.D.**

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be necessary to keep this problem under control. Furthermore, once the fused-silica furnace walls are coated with W they become opaque. IR radiation from the heating coils is no longer transmitted as efficiently through the walls as when the fused silica is transparent. Hence, temperature control of the wafers becomes a problem. Note that in cold-wall reactors, the wafers and their holders are the only hot objects in the chamber, with the wall temperatures being kept well below the temperature needed to drive the deposition reactions ($<150^{\circ}\text{C}$). Thus, the problem of deposition on the chamber walls is curtailed (but note, not entirely eliminated). However, a large temperature gradient exists between the heated wafers and the chamber walls, which may also create temperature control difficulties in such reactors.

6.7.1.2 Blanket CVD W and Etchback: Tungsten can be deposited by CVD using either a selective or blanket process. Only blanket-W deposition has emerged as a production-proven process, despite the fact that it is more complex and expensive than selective CVD-W. Acceptance of the selective-CVD process has been slowed because some of its problems have not been completely overcome, including those involving loss of selectivity of deposition and lateral encroachment and wormholes. On the other hand, blanket CVD-W and etchback (or CMP) has found widespread use for contact-hole and via filling applications in IC technologies below about $1\text{ }\mu\text{m}$. Both applications require adherent, low-cost films. The plug applications, however, call for high step-coverage and thickness uniformity, but can tolerate higher resistivity than is needed for W-films used as interconnects. For filling contact holes this W-plug-formation process has six steps:

1. *In situ* surface pre-clean;
2. Deposition of a contact forming layer (typically a Ti film formed by sputtering or CVD);
3. Deposition of an adhesion/barrier layer (typically a TiN film formed by sputtering or CVD);
4. Blanket-CVD of the W film (typically a two-step deposition process);
5. Etchback of the W film;
6. Etchback of the adhesion and contact-forming layers.

The surface pre-cleaning step is designed to remove any native SiO_2 material on the silicon in the contact holes or aluminum oxide on the aluminum in vias. Trends are moving toward making this an *in situ* cleaning step, so that the wafer surface is not exposed to atmosphere between the cleaning step and the deposition of the contact and adhesion layers. Most such *in situ* processes involve either an Ar sputter clean (discussed in Chap. 11) or a "soft" plasma clean. After the cleaning step, the contact and adhesion layers are deposited, either by CVD or sputter deposition. Currently, the most widely used materials for the contact and adhesion layers are Ti and TiN, respectively. The thin layer of Ti (30–50 nm thick) is used under the TiN adhesion layer because it provides lower contact resistance to the silicon substrate than is possible with TiN.¹⁰⁰ The adhesion layer is needed because of the extremely poor adhesion of CVD W to such insulators as BPSG, thermal oxide, plasma-enhanced oxide and plasma-enhanced silicon nitride. Tungsten, however, adheres well to TiN, and TiN in turn, adheres well to these insulators. Thus, a method which allows good adhesion of CVD-W to the substrate is

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achieved.* A detailed discussion of depositing these layers is provided in later sections of this chapter, and etching of the W and TiN is described in Chap. 14.

Next a layer of CVD-W is blanket deposited. For the W-plug applications the contact holes or vias must be completely filled. For this to occur the step coverage (in this case, defined as the ratio of the thickness at the sidewall at half depth of the hole to that of the nominal W thickness on the wafer surface) must be 100%. Otherwise, keyholes, or voids, will be formed (Fig. 6-47a), and these voids will become exposed during the subsequent W etchback step. If that happens, the contact holes or vias are no longer completely filled at the end of the W-plug formation process. In general, the hydrogen reduction gives better step coverage than the silane reduction, although the deposition rate of the former is significantly lower. However, W layers formed by the hydrogen reduction do not nucleate reliably on the TiN adhesion layers. So, in most commercial reactors a two-step blanket-W process is typically employed.^{78,81} A thin layer of W is first nucleated using the silane reduction (several tens of nm thick). Then, the hydrogen reduction reaction is used to deposit the remainder of the blanket-W film. The silane reduction step is carried out at relatively low pressures (~1 torr), while the hydrogen reduction uses higher pressures (25–80 torr). Such higher chamber pressures during the hydrogen reduction process significantly improve the step coverage and produce void-free filled contact holes and vias (Fig. 6-47b). As described in Chap. 3, the total chamber pressure is increased by throttling the pumping speed. The process is run at temperatures around 450°C, where the deposition still operates in the surface-reaction-rate-limited regime. Details of the higher-pressure hydrogen-reduction deposition process are given in Ref. 78. To get complete filling of the contact holes or vias, the slope of the contact sidewalls should not exceed 90°. A blanket-W process using SiH_2F_2 and WF_6 as the reactants has also been studied and the results published, with some advantages claimed over the hydrogen reduction process.⁸²

* TiN has been reported to have the best set of properties for this adhesion/barrier-layer application, and the best resistance to the etch gases used to etchback the CVD W.

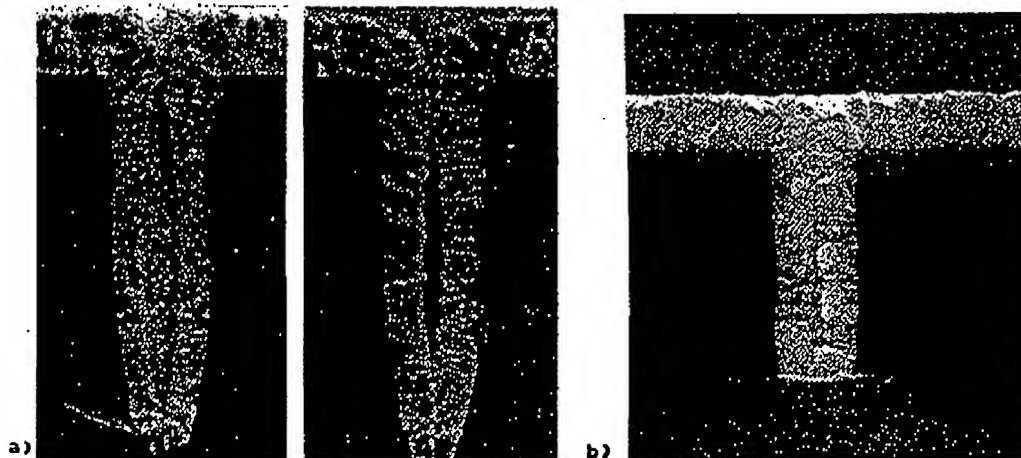


FIG. 6-47 a) Blanket-CVD W films deposited into a trench with a process that results in voids.⁸³ b) A blanket CVD W film deposited into a trench without void formation.

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contact holes and vias. As mentioned earlier, films that are required to perform both adhesion and diffusion-barrier functions are also termed *liners*. The deposition of liner films is done by either PVD or CVD. PVD technology has been the traditional deposition method, and work to improve this method continues. However, as shall be discussed in detail in Chap. 11 (and briefly here), CVD and *ion metal plasma* (IMP) PVD offer potentially better step coverage over sharp upper edges of contacts and at the bottom corners of deep submicron contacts and vias. Here we discuss the CVD of the most widely used liner film *titanium nitride* (TiN).

TiN is an attractive material as a diffusion barrier in silicon ICs because it behaves not only as an impermeable barrier to silicon, but also as a barrier to other substances attempting to diffuse through it. In the latter cases, the activation energy for the diffusion of other impurities in TiN is high (e.g., the activation energy for Cu diffusion into TiN thin films is 4.3 eV, whereas the normal value for diffusion of Cu into metals is only 1 to 2 eV). TiN is also chemically and thermodynamically very stable (its melting point is 2950°C), and when in thin film form it exhibit one of the lowest electrical resistivities (25-75 $\mu\Omega\text{-cm}$) of the transition metal carbides, borides, and nitrides.

The specific contact resistivity of TiN films to Si is somewhat higher than that of Ti ($\sim 10 \mu\Omega\text{-cm}^2$), and as a result TiN is ordinarily not used to make direct contact to Si. As discussed earlier, it is commonly used in contact structures together with an underlying layer of Ti (TiN/Ti/Si). Such contact structures exhibit very low specific contact resistivities to Si and remarkably high thermal stability. However, if a conventional reactive sputtering process is used to deposit TiN into high-aspect ratio recesses, an overhang of TiN is formed at the top corners of the contact. If too thick a layer of TiN is deposited, this overhang can eventually close off the hole and form a keyhole. Even if such a deposition is not allowed to proceed to the point of hole closure, the overhang shadows the bottom corners of the contact hole, and thinning of the liner film occurs there (Fig. 6-53a). Furthermore, since liner films like TiN form a columnar polycrystalline structure when deposited by PVD, a grain boundary is likely to be formed at the lower corners, where the film is already thinnest. The short, high-speed diffusion paths at these

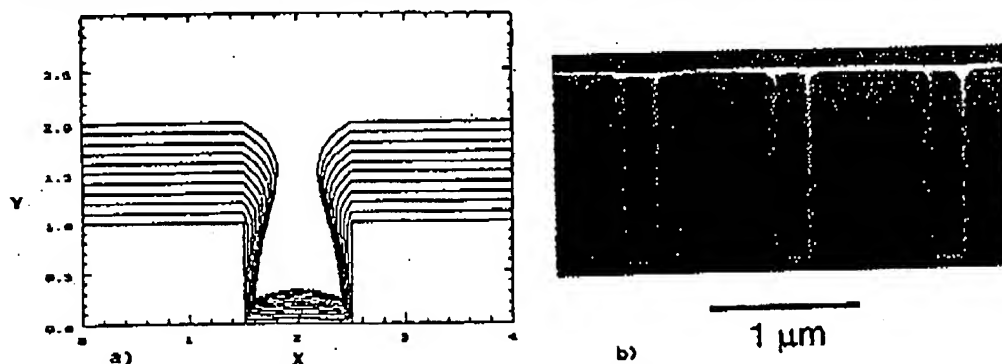


Fig. 6-53 a) Simulation of sputter deposition of a film (e.g., TiN) into a contact hole showing the formation of an overhang at the top corners of the contact, and thinning at the bottom corners. b) Deposition of TiN by CVD showing conformal coverage.⁹³ Reprinted with permission of the Electrochemical Society.

MULTI-LEVEL INTERCONNECTS FOR ULSI 723

have a finer pitch, and therefore higher resistance and capacitance) should be reserved for interconnecting neighboring devices with short interconnection lines. The upper interconnect levels, which are usually designed with a larger pitch and lower resistance, should be used to transmit signals across the entire chip.

15.1.1.3 Cost: If multilevel-interconnect processes are used to fabricate integrated circuits, the die size should decrease. Thus, more die per wafer can be manufactured. If the manufacturing cost per wafer remains the same and the yield is not impacted by the implementation of a multilevel-interconnect process, the cost per chip will decrease. In fact, smaller die sizes should imply higher yields, and enhancing the benefit of chip-size reduction. In addition, improved device performance may allow the circuit to command a higher market price.

However, the implementation of a multilevel-interconnect system requires that at least two additional masking steps be used for each additional level of interconnect. The extra process steps add to the manufacturing cost of each wafer. The number of defects/cm² is also generally proportional to the number of masking steps. In addition, the manufacturing yield and long-term reliability for a multilevel metal process are typically lower, since the process becomes more technically demanding. As a result, it must be determined whether the chip-size reduction and enhanced chip value will produce a margin of profit that is greater than the amount lost due to additional incurred process costs and yield and reliability loss.

15.1.2 Problems Associated with Multilevel-Interconnect Processes

As alluded to previously, adding a multilevel interconnect process to a fabrication sequence introduces a new set of difficulties. In addition to added process complexity and loss of topological planarity, there are several other concerns.

First, new materials must be used, which necessarily involves an extensive characterization of their properties to ensure they are compatible with all other aspects of the process technology. Second, new process-related manufacturing difficulties may be encountered that can adversely impact manufacturing yield (e.g., interlevel shorts due to pinholes; stringers due to incomplete etching over severe steps; failure to open vias due to difficulty in implementing reliable endpoint-detection techniques in the dry-etch process; film delamination due to poor adhesion or high stress; and difficulty in bonding to some metal alloys). Third, new failure modes may be encountered. For example, electromigration, corrosion, and hillock formation, which must also be characterized to determine whether they will significantly compromise circuit reliability.

The problems related to multilevel interconnects are listed at this point in order to show that benefits can be gained only by successfully pursuing a considerable technical-development effort. More specific details on these problems (and how they can be overcome) will be provided throughout the chapter.

15.1.3 Terminology of Multilevel-Interconnect Structures

Figure 15-3 shows the terminology associated with a double-level-metal structure for MOS technologies. The MOS structure has a dielectric layer between the polysilicon gate/interconnect level and Metal 1, which is referred to as the *pre-metal dielectric* (or *PMD*). The dielectric

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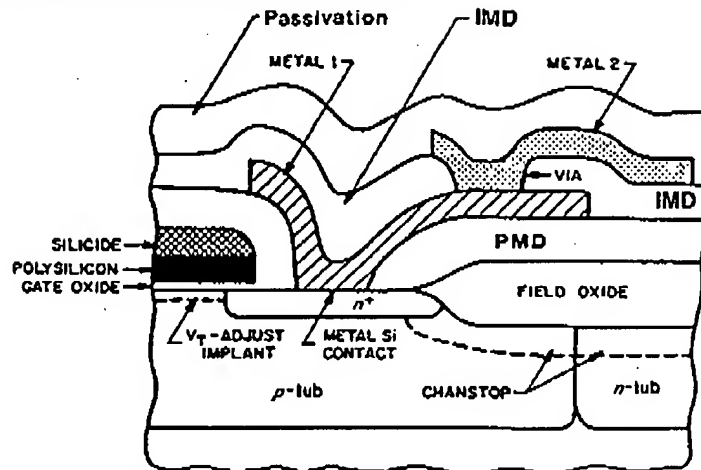


Fig. 15-3 Terminology of double-level metal interconnects.

layers between metal levels are called *intermetal dielectrics (IMD)*. The openings in PMD are referred to as *contact holes* (or *contacts*). They allow electrical connections to be established between Metal 1 and polysilicon, as well as between Metal 1 and the Si substrate. Openings in the intermetal dielectric layers are known as *vias*: these allow contact to be made between Metals 1 and 2, Metals 2 and 3, etc.

In bipolar technology, the dielectric layer between Metal 1 and the substrate is still referred to as PMD, despite the fact that it may not isolate Metal 1 from polysilicon. The openings in PMD are again called contact holes, although they are only used to allow contact to be established between Metal 1 and the substrate (i.e., not poly). The notation for the other metal and dielectric layers is otherwise identical to that used in MOS technologies.

A distinction exists between the use of the terms *multi-level* and *multilayer*. A *multilayer-interconnect* structure is a thin film consisting of more than one layer of material, but existing at just one level of the interconnect system. Hence, a multilayer film can serve as the conductor (or dielectric) at each level of a multilevel-interconnect system.

15.2 MATERIALS FOR MULTILEVEL INTERCONNECT TECHNOLOGIES

The two groups of materials employed in multilevel-interconnect technologies are thin-film conductors and thin-film insulators. In this section the properties of materials that have been adopted for use in ULSI applications will be described.

15.2.1 Conductor Materials for Multilevel Interconnects

There are a variety of conductor materials used in the interconnect structure of ICs. Aluminum and aluminum alloys (e.g., Al-Si, Al-Cu, and Al-Si-Cu) have been the most widely used metals. Their properties and deposition method (sputtering) are described in Chap. 11. Heavily-doped polysilicon has also been employed, primarily as a local interconnect. This material is discussed in Chap. 6. Polysilicon with an overlaid metal silicide layer (to reduce the resistance) is also used (with WSi_2 , TiSi_2 , and CoSi_2 being the materials utilized in such *polycide* structures).

MICROCHIP MANUFACTURING

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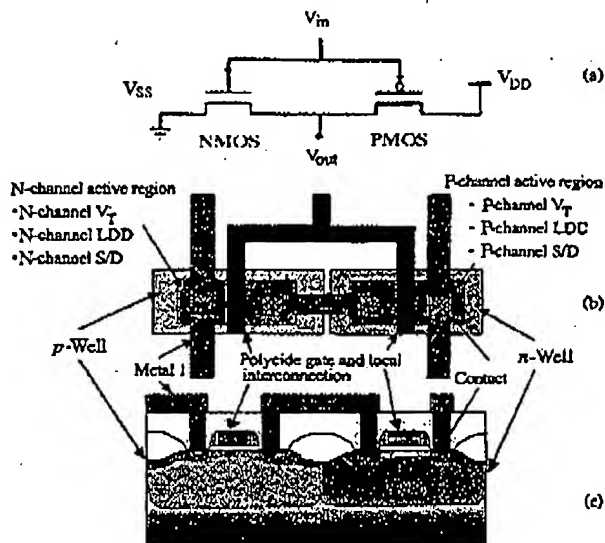


Fig. 4-7 CMOS inverter: (a) Circuit-diagram form; (b) Layout form; and (c) Physical form (in cross-section).

tion is ready to be used to generate a set of masks that will serve as tools for specifying the circuit-patterns on silicon-wafers. This layout information is stored on a computer. A photograph of a completed (unpack-

aged) IC is shown in Fig. 4-9.

In this book the details of the integrated-circuit manufacturing steps summarized in Fig. 4-2 are discussed. These steps start when the *layout-information* has been finalized. At that point procedures are utilized to convert the layout-information stored on the computer, into a set of *masks* or *reticles*. This procedure is described in Chap. 20. The individual fabrication process-modules associated with creating-patterns, introducing-dopants, and depositing-films on silicon-substrates (to form the integrated-circuit features) are also subjects of this volume.

In this chapter, information is presented about how such individual process-modules are combined to create a complete CMOS chip (a subject referred to as *process-integration*).^{1,2} Note that examples of process-flows for fabricating bipolar and NMOS ICs are given in Chap. 3 (see Figs. 3-15 and 3-19, respectively). The CMOS-inverter shown in Fig. 4-7 can be used as an example of the type of IC-structure created by such a CMOS process-flow. In this figure, the CMOS-inverter is represented in several ways. First, it is shown in its *circuit-schematic* form (Fig. 4-7a). Next the layout of the completed CMOS-inverter is

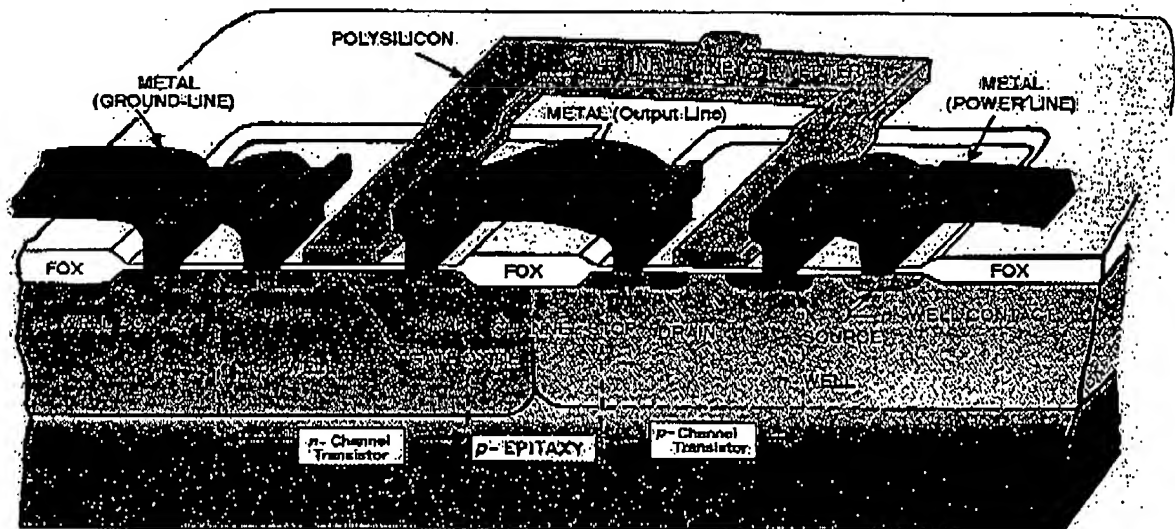


Fig. 4-8 Perspective-view of an inverter logic-gate fabricated using a twin-well CMOS technology.

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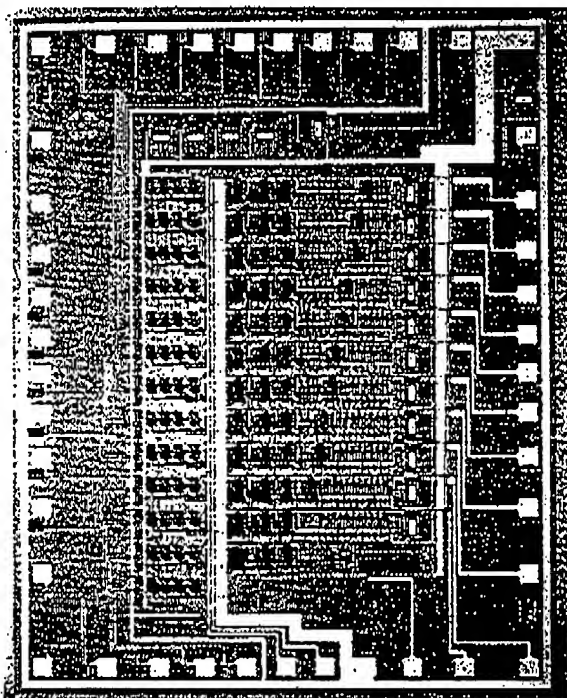


Fig. 4-9 Photograph of a completed IC-chip (unpackaged).

given (Fig. 4-7b). Then a *cross-sectional view* of the inverter structure on an IC-chip is depicted (Fig. 4-7c). It is this cross-sectional form that will be used to step through the *CMOS process-flow*. Finally, Fig. 4-8 depicts a *perspective-view* of such a CMOS-inverter IC-structure. This view includes the isolation-structures, power-lines, signal-lines, and contacts to the silicon-substrate needed in CMOS.

4.2 CMOS PROCESS-FLOW

A modern CMOS-IC process-flow involves 350 (or more) process steps and may take six-to-eight weeks to complete. The process-flow is a sequence of the chemical and physical operations that are performed on the silicon-wafer.

Here we present a 15-mask, twin-well, 2-level-metal CMOS process-flow. (Details about each of the individual processes are given in later chapters.) This flow is representative of process sequences used to fabricate CMOS-ICs from 1.2- μm down to about

0.35- μm . It provides an overview of the series of steps employed in fabricating such CMOS-ICs. A cross-section (at completion of Metal-1 processing) using this process-flow is shown in Fig. 4-7c.

Twin-well CMOS-technology is used for CMOS generations below 1- μm because two separate-wells can be formed in the lightly-doped substrate region. Well-profiles can be tailored independently so that neither device suffers from excessive-doping effects.

Note that in this process-flow, LOCOS-isolation is used (defined in Sect. 4.2.2). In more advanced ICs (i.e., for CMOS-technologies of 0.25- μm and smaller), an alternative isolation approach, namely *shallow-trench-isolation* (STI), is implemented. The details of forming such STI-structures is described in Sect. 4.3.

4.2.1 Starting Material for CMOS-ICs

All MOS technologies use silicon-wafers with a $\langle 100 \rangle$ -orientation. Typically, in twin-well CMOS the starting material is also either a lightly *p*-doped wafer (*p*-bulk-wafer), or a heavily *p*-doped wafer on which a thin, lightly *p*-doped epi-layer is grown (Figs. 4-10a and 10b, respectively). The concentration range of the *p*-doping in both the bulk-wafer and the surface *p*-epi

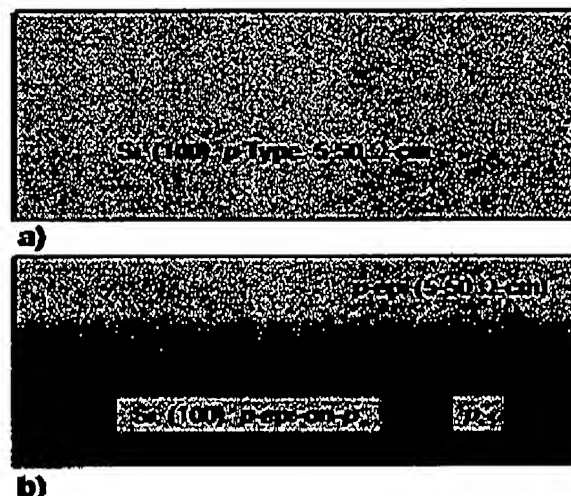


Fig. 4-10 Silicon starting substrates for twin-well CMOS: (a) *p*-bulk wafer; (b) *p*-epi-on-*p*⁺ wafer.

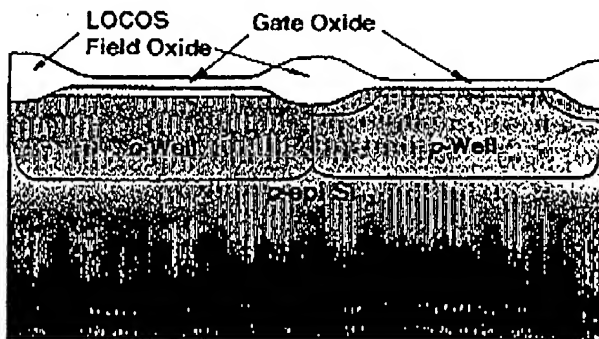


Fig. 4-22 The silicon wafer surface after: (a) etching back the pad-oxide to bare silicon; and (b) growing the gate-oxide.

performed sequentially using the same implanter, along with the NMOSFET V_T -adjust implant.

4.2.5 Gate-Oxide Growth

In the next step, the gate-oxide is formed. The growth of the gate-oxide is critical. A defect-free, very-thin (6-20-nm), high-quality oxide without contamination is essential for proper device operation. The gate-oxide is grown only on the exposed active-regions (following a careful cleaning of the wafer surface just prior to an oxide growth-process in dry- O_2).

Since the drain-current in an MOS transistor is inversely proportional to the gate-oxide thickness

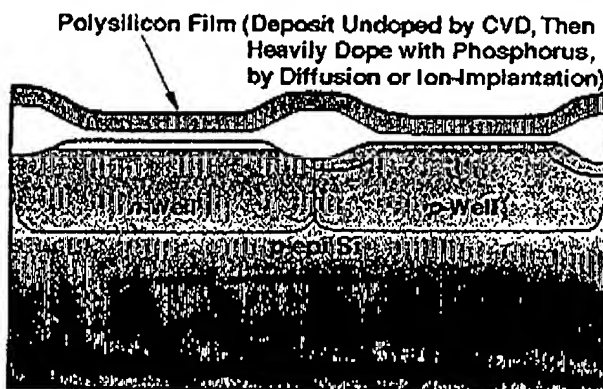


Fig. 4-23 A layer of undoped-polysilicon is next blanket-deposited using LPCVD. Diffusion or ion-implantation is used to heavily-dope the polySi layer with phosphorus.

(for a given set of terminal voltages), the gate-oxide is normally made as thin as possible (commensurate with oxide-breakdown and reliability considerations). For the 0.35-1.0- μm generations of CMOS, the gate-oxide used is 10-20-nm thick. (See Chap. 13 for details on thin gate-oxide growth.) The wafer after this gate-oxide growth process is shown in Fig. 4-22.

4.2.6 Polysilicon-Deposition and Patterning

Once the gate-oxidation step is completed, a heavily n -doped polysilicon-gate structure is fabricated. Polysilicon is the preferred gate material for several reasons. First, it can withstand the high-temperature steps required to form the source/drain junctions. Second, the poly/ SiO_2 interface is well understood and electrically stable. The gate-formation procedure begins with the deposition of a 0.4-0.5- μm -thick, undoped polysilicon-film by LPCVD (Fig. 4-23, see also Chap. 16). This layer is then doped with phosphorus by ion-implantation or chemical-doping, producing a film with a sheet resistance of 20-30- Ω/sq .

The gate-structure (and polysilicon-interconnect-structures) are then patterned using Mask #6. Following exposure and development of the resist, the polysilicon-film is dry-etched (Fig. 4-24). This is also a critical etch-step for several reasons. First, due to the self-aligned nature of silicon-gate technology,

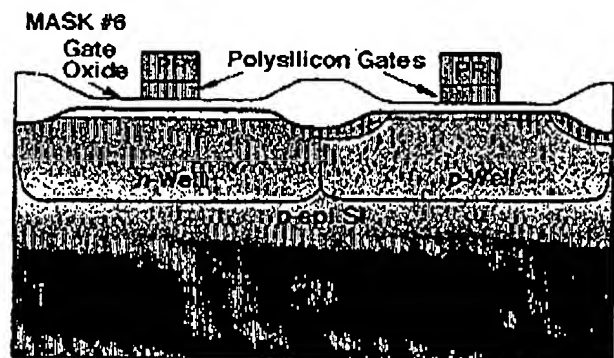


Fig. 4-24 Photoresist is applied, and Mask #6 is used to define the gates of the MOSFETs in the polysilicon-film. An anisotropic polySi dry-etch-step defines their gatelength. Following this etch, the resist is stripped.

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the channel-length of the device depends on the width of the polysilicon-line. Hence, the gate-length dimension must be precisely maintained across the entire wafer (and from wafer-to-wafer). If the gate-length is too long, the drain-current of the MOSFETs will decrease, slowing-down the performance of the IC. If the gate-length is too short, the source and drain may *punch-through*. In addition, the profile of the etched poly-gate structure should be vertical. This prevents variation of channel-lengths (due to penetration of the ions of the thinner regions of the gate sidewalls during formation of the source/drain regions by ion-implantation). Finally, to achieve the above goals, an anisotropic polysilicon-etch-process must be employed. This process, however, requires overetching to remove the locally thicker regions of polysilicon that exist wherever it crosses steps on the wafer surface (see Fig. 22-13). During this *overetch-time*, areas of the thin gate-oxide are exposed to the etchants. Thus, it is necessary to use a polysilicon etch-process that is highly-selective with respect to SiO_2 (see Chap. 22).

4.2.7 Formation of Source/Drain Regions

The next step in the process-flow is the formation of source and drain (S/D) regions of the MOSFETs. Such regions are paths of current-flow in the silicon

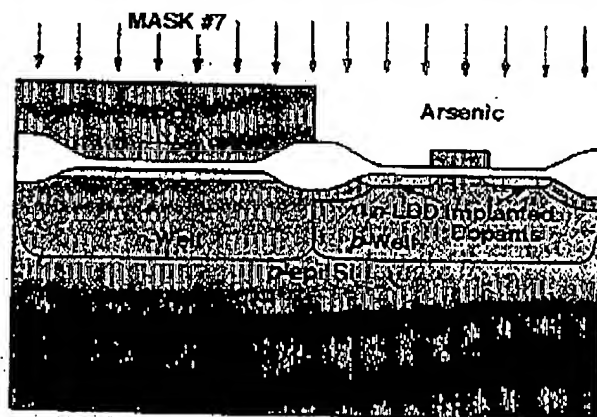


Fig. 4-25 Photoresist is applied, and *Mask #7* is used to cover the regions where PMOSFETs exist. A shallow arsenic-implant provides the doping for the *lightly-doped-drain (LDD)* regions of the NMOSFETs.

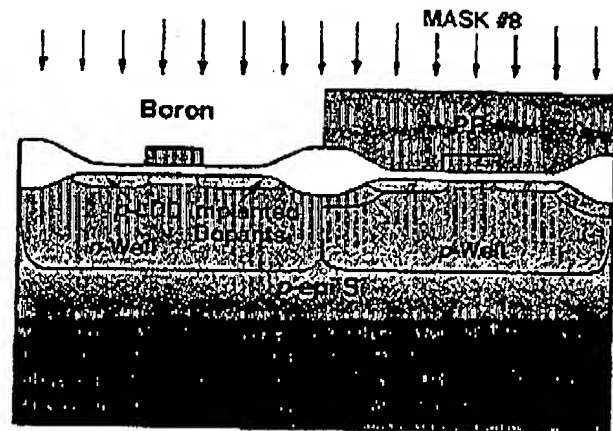


Fig. 4-26 Photoresist is applied, and *Mask #8* is used to cover the regions where NMOSFETs exist. A shallow boron-implant provides the doping for the *lightly-doped-drain (LDD)* regions of the PMOSFETs.

between the metal interconnect-lines and the channel of the transistor. As such, it is important that they have the lowest possible resistance. In addition, submicron-MOSFETs require S/D junctions to be as shallow as possible to suppress such short-channel effects as punchthrough (see Ref. 2). To obtain low resistivity, the S/D regions are doped as heavily as possible (typically using ion-implantation, with a dose on the order of $\sim 10^{15} \text{ cm}^{-3}$). The NMOS S/D regions are doped with arsenic because it has a high-solubility, low-diffusivity, and a shallow projected-range at the low ion-implantation energies that are used. Boron or BF_2^+ are used to dope the PMOSFET S/D regions. However, boron has a higher-diffusivity in Si than does arsenic. Hence, shallow S/D-junctions in PMOSFETs are harder to achieve than in NMOSFETs.

In submicron-CMOS processes, gate-lengths become so small that *lightly-doped-drain (LDD)* structures must be used to minimize hot-electron effects, especially in NMOS devices. Thus, procedures are integrated into the CMOS process-flow to fabricate such LDD-structures. If LDD-structures are needed for both PMOS and NMOS devices, two more masking-layers are needed.

The LDD-structures are formed in the follow-

ing way. Resist is spun on, and *Mask #7* is used to protect all the devices except the NMOS-transistors (Fig. 4-25). The lightly-doped regions of the NMOS source and drain are created with an ion-implant step. Arsenic at a dose of approximately 3×10^{13} – 3×10^{14} cm^{-2} dopant-ions is implanted at low-energy (30–50-keV). The implant-process causes the edge of these implanted ions to be automatically aligned to the edge of the gate (i.e., it is a *self-aligned process*).

The resist is stripped and a new layer of resist is spun-on, and *Mask #8* is used to protect all the devices except the NMOS transistors (Fig. 4-26). The lightly-doped regions of the PMOS source and drain are created with an ion-implant step. Boron at a dose of between 3×10^{13} – 3×10^{14} cm^{-2} ions is implanted at low-energy (30–50-keV), and the resist is stripped.

A conformal layer of dielectric material (usually SiO_2 or silicon-nitride) is then deposited over the entire wafer (Fig. 4-27). An anisotropic-etch process is used to clear the oxide in the flat areas while leaving *spacers* on the sidewalls of the poly gates (Fig. 4-28). These spacers cover and protect the regions beneath them from the subsequent *high-dose implants* that form the rest of the S/D regions.

A photoresist layer and *Mask #9* is used to define the areas where the heavily-doped regions of the NMOS source and drain will be located. (Figure 4-29). These are formed with a heavy-dose arsenic implant-step (dose = 2×10^{15} – 4×10^{15} As-ions/ cm^2 at 40–80-keV). A photoresist layer and *Mask #10* is then

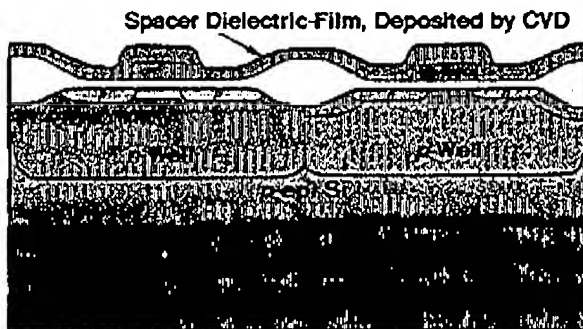


Fig. 4-27 A conformal layer of SiO_2 or SiN is deposited by CVD in preparation for the sidewall-spacer formation.

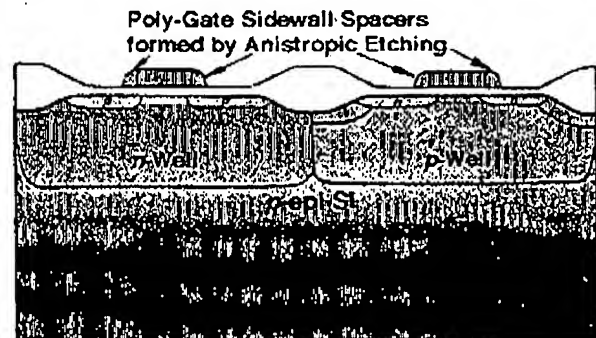


Fig. 4-28 The deposited dielectric-layer is etched-back anisotropically, leaving sidewall-spacers along the edges of the polysilicon gate-structures.

used to define the areas where heavily-doped PMOS source/drain regions will be located (Figure 4-30). These are formed with a heavy-dose boron implant-step (dose = 1×10^{15} – 3×10^{15} B-ions/ cm^2 at 50-keV).

In the final step of the active-device formation process, a furnace anneal (typically at $\sim 900^\circ\text{C}$ for 30 min, or a rapid-thermal-anneal [RTA] for ~ 1 min at 1000 – 1050°C) is carried out. This thermal-step activates all the implants, anneals the implant-damage, and drives the junctions to their final depths.

4.2.8 Formation of TiSi_2 Salicide

After stripping the thin-oxide on the active-Si regions and cleaning the wafer surface (to ensure that no

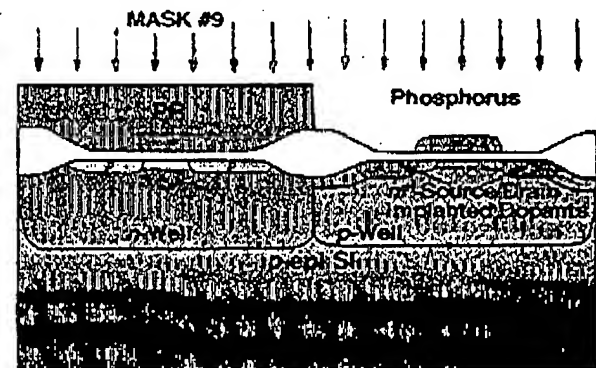


Fig. 4-29 After applying resist, *Mask #9* is used to cover the regions with PMOSFETs. A phosphorus-implant is used to form the n^+ -source/drain regions of the NMOSFETs.

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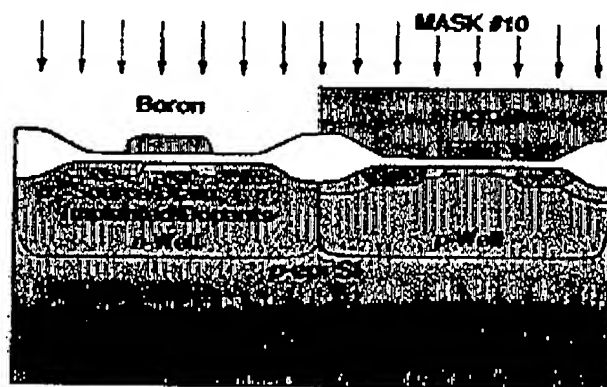


Fig. 4-30 After applying resist, Mask #10 is used to cover the regions with NMOSFETs. A boron-implant is then used to form the p^+ -source/drain regions of the PMOSFETs.

native-oxide exists on the exposed silicon of the active regions and on the polysilicon-gates, Fig. 4-31), a thin-layer of titanium (Ti) is deposited by sputtering (50-100-nm thick, Fig. 4-32). The next step makes use of two chemical reactions. The wafers are first heated to 600°C in an N_2 -ambient for a short time (about 1-min). At this temperature, the Ti reacts with Si where they are in contact to form $TiSi_2$. $TiSi_2$ forms a low-resistance-contact to silicon, and it is also an excellent conductor. The wafer is then immersed in a solution of $NH_4OH:H_2O_2:H_2O$ (1:1:5) to selectively remove the unreacted Ti (i.e., on regions of the wafer covered with SiO_2), but the $TiSi_2$ remains in regions over Si where it had reacted (Fig. 4-33). After this

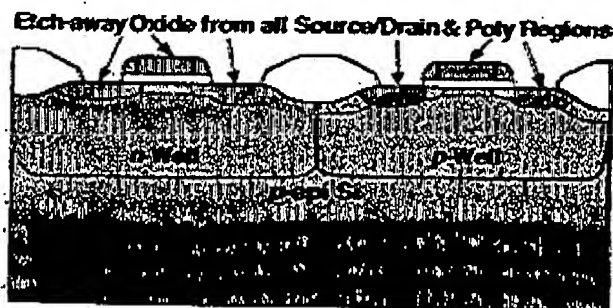


Fig. 4-31 An etch-step is used to remove the thin-oxide layer that covers the source/drain and gate-poly regions of all MOSFETs, in preparation for salicide formation.

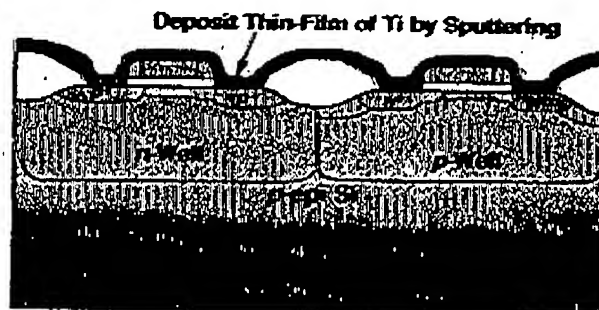


Fig. 4-32 A thin-layer of titanium (Ti) is blanket-deposited over the wafer-surface by sputtering.

Ti-etch-step, the wafer is heated to 800°C for about 1-minute in N_2 (to reduce the resistivity of the $TiSi_2$ -layer to its final value of $\sim 1 \Omega/sq$). Figure 4-34 shows the details of the *Ti-salicide* formation process.^{5,6}

4.2.9 Premetal-Oxide Deposition and Planarization, and Contact-Formation

Following formation of the source and drain regions and the Ti-salicide structure, a doped dielectric-film is deposited by CVD. This layer is known as an *interlevel dielectric* (ILD). Contact-windows are opened in this dielectric-layer to allow electrical connections to be made between Metal-1 and the following structures:



Fig. 4-33 A lower-temperature anneal-step (600°C, 1-min RTP in N_2) converts the Ti to $TiSi_2$ on regions where Ti is contact with Si. Elsewhere, Ti does not react, and can therefore be selectively removed with a wet-etch step. A second, higher-temperature anneal-step (800°C, 1-min RTP in N_2) converts the $TiSi_2$ to its final, lower-resistance form.

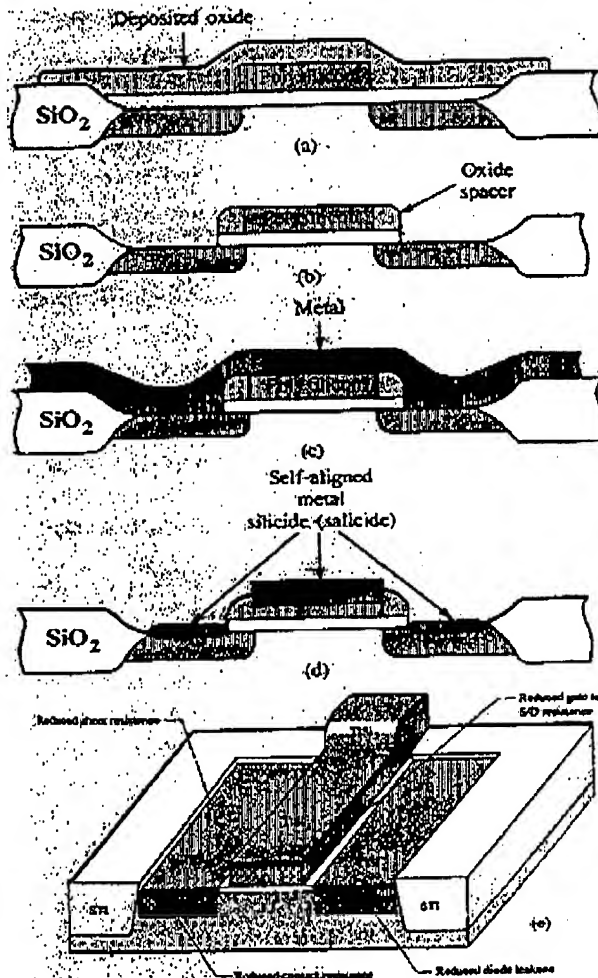


Fig. 4-34 Process sequence used to form titanium-salicide: (a) Form the standard MOSFET structure up to source and drain; (b) Form sidewall-spacers; (c) Deposit Ti-film and react to form TiSi_2 in regions where Ti is in contact with Si; (d) Selectively remove unreacted Ti film; (e) a perspective drawing of the final salicide-structure.

1) source/drain contact regions; 2) gate contacts; 3) substrate-contact regions; and 4) well-contact regions. A CVD-process is used to deposit this doped SiO_2 -film (about $1\text{-}\mu\text{m}$ thick), onto the wafers (see Chap. 16 for details of this process). The dopant in the SiO_2

Deposit Inter-Level-Dielectric (ILD) Layer by CVD, Then Planarize this Layer with Oxide-CMP Process

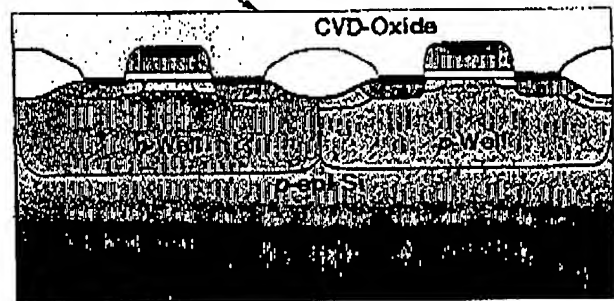


Fig. 4-35 A conformal interlevel-dielectric layer (typically CVD- SiO_2) is deposited. Then chemical-mechanical polishing (CMP) is used to planarize the steps of the ILD.

is either phosphorus (P - in which case the material is referred to as *phosphosilicate glass* or *PSG*), or both P and B (*borophosphosilicate glass* or *BPSG*).

The doped CVD SiO_2 -layer plays several roles in the fabrication and operating aspects of the circuit. First, it acts as an *insulating-layer* between polySi and Metal-1. Second, it reduces the *parasitic-capacitance* between Metal-1 and the substrate. Third, adding P to the glass makes the layer an *excellent getter* of Na ions (contamination by Na can destabilize the V_T of a MOSFET). The PSG (or BPSG) binds otherwise mobile Na-atoms in the doped-glass layer, preventing them from reaching the gate-oxide and altering V_T .

Note that the surface of the wafer after the ILD deposition is highly nonplanar. For the sake of reducing potential problems with metal discontinuities, it would be preferable not to deposit the metal directly on such rough topography. To avoid having to do this, a variety of techniques were developed to *planarize* (or flatten) this topography, including *BPSG-reflow* (see Chap. 16).

However, the method that provides the highest level of planarity is *chemical-mechanical polishing* (CMP), and is described here (see also Chap. 23). The ILD-layer is deposited thicker than the largest steps present on the wafer surface (that is, thicker than $\sim 1\text{-}\mu\text{m}$). The wafer is then placed face-down in a CMP-tool, and its upper-surface is polished-flat using

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a high-pH silica-slurry. This CMP-process results in a structure that is shown in Fig. 4-35.

Contact-openings are next created by a lithography-and-etch step (Fig. 4-36). After applying resist, *Mask #11* is used to define contact-patterns in a photo-resist-film. A dry-etch process is then used to open the contact-windows through the ILD to the underlying polySi and the source/drain regions in the silicon.

This contact-opening step can be critical, as the contact size and its alignment to underlying patterns limit the minimum-size of the device. The source/drain regions must also be large enough for the contact to fit, with an allowance for alignment tolerance. If the contact opening exposes a part of the substrate, the drain or source will be shorted to it. Likewise, if the contact-opening overlaps the both the source/drain and the gate, a short will be created between them.

4.2.10 Metal-1 Deposition and Patterning

After the contacts have been opened, the metallization layer is deposited. Because the metal-layer is highly conductive, it is used whenever possible to interconnect circuit-elements and to carry large amounts of supply-current. Metal interconnect-lines must have sufficient thickness, width, and step-coverage to keep the current-density in each line below the level that

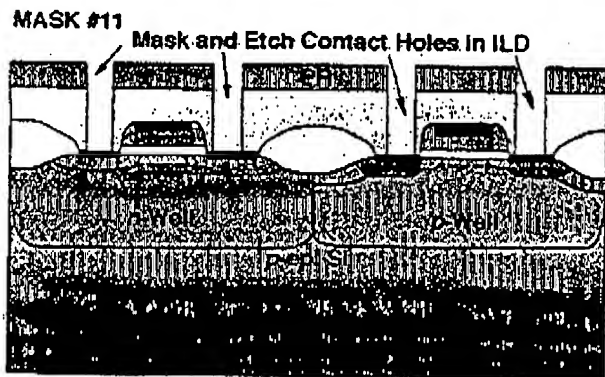


Fig. 4-36 After applying resist, *Mask #11* is used to pattern the contact-opening regions. A dry-etch step is used to anisotropically etch the ILD layer to allow connections to be made to the silicon-substrate (and polysilicon layers).

Deposit TiN-liner by PVD, and W-film by CVD

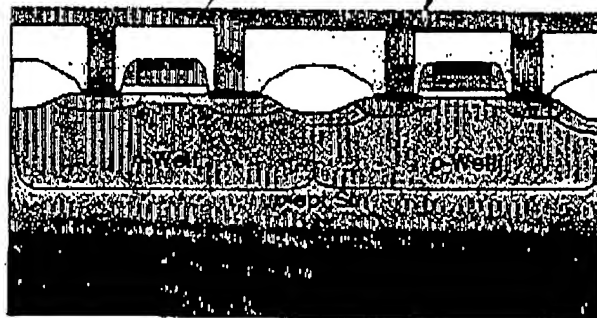


Fig. 4-37 To form the tungsten-contact holes, an adhesion-layer of titanium-nitride (TiN) is first blanket-sputter-deposited onto the wafer. Then a CVD-process is used to blanket-deposit a film of tungsten. This W-film completely fills the contact-holes.

could produce electromigration failure (see Ref. 2). In addition, the space between adjacent metal-lines must be large enough so that the lines never touch, even under worst-case process variations.

The metallization-structure is formed using two separate processes: 1) *W-plug formation*; and 2) *main interconnect-line formation*, using an Al:Cu film. In the W-plug formation-process a thin barrier/glue layer of Ti/TiN is first blanket-deposited by sputtering (a few tens-of-nm thick). It provides good adhesion to the SiO_2 and other underlying materials, as well as serving as an effective barrier-layer between the upper and lower metal-layers. The next step is deposition of a blanket-W layer by CVD, as shown in Fig. 4-37. CMP is then used to planarize the wafer surface, and to remove the W and Ti/TiN everywhere but in the contact-holes. Thus, W-plugs are formed, as shown in Fig. 4-38.

The main-interconnect lines are formed from Al:Cu-alloy films that are deposited next by sputtering. A resist-layer and *Mask #12* are used to define these main interconnect-line patterns (Fig. 4-39), which are then formed using a dry-etching process (Fig. 4-40). Note that Cu is replacing Al:Cu in some of the most advanced IC-technologies, because of its higher-conductivity and better electromigration resis-

Form W-plugs by Using CMP to Remove the W-film and the TiN film on the Top ILD Surface

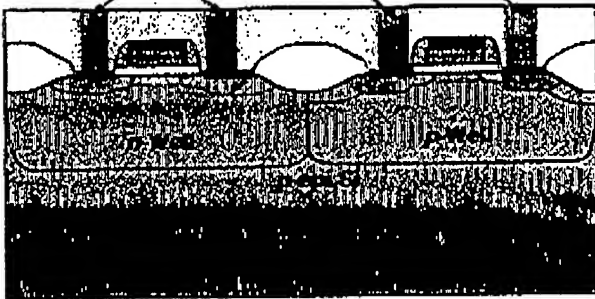


Fig. 4-38 The W and TiN that is deposited on the top surface of the ILD is removed by a CMP process, leaving just W-plugs.

tance (see Chap. 24). Figure 4-41 shows a SEM of Al:Cu-interconnect-lines (Metal-1) and W-plugs.

If a single-level of metal is used in the CMOS process, a *sintering-step* occurs after the metal has been patterned. This step brings the metal and the n^+ and p^+ regions in the silicon into intimate contact. Such intimate contact between the metal and the heavily-doped Si regions establishes low-resistance ohmic contacts. The annealing-process also exposes the wafer to a 375–500°C temperature in an H_2 or $N_2 + H_2$ (5%) ambient for about 30 minutes. This step also serves as the annealing-process for reducing the

MASK #12 Deposit Al:Cu Alloy Film and Mask It

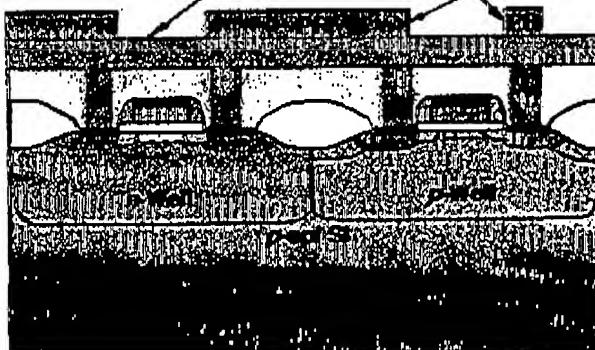


Fig. 4-39 An Al:Cu alloy film is sputter deposited onto the wafer. Photoresist is applied and Mask #12 is used to define the Metal-1 lines that be formed from the Al:Cu film.

Etch Al:Cu Alloy Film and Strip Resist

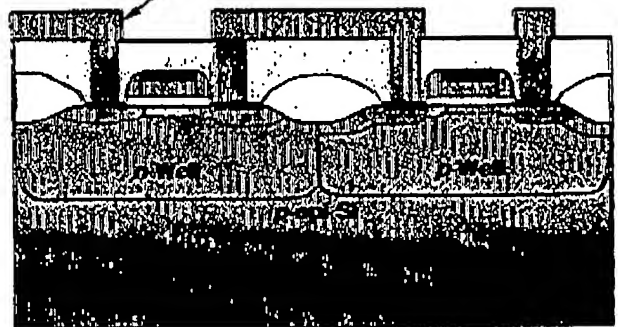


Fig. 4-40 The Al:Cu Metal-1 lines are created by using an anisotropic Al dry-etch process. The resist then stripped.

interface-trap-density in the gate-oxide that was introduced by earlier processing steps (see Chap. 13).

4.2.11 Intermetal-Dielectric Deposition, Via-Patterning, and Metal-2 Deposition and Etch

Most modern ULSI technologies use more than one level of wiring on the wafer surface. This is because in complex circuits it is usually very difficult to completely interconnect all the devices in the circuit without using multiple interconnect-levels. The processes used to deposit and define each level are similar to those we described for Metal-1. Here we show a two-

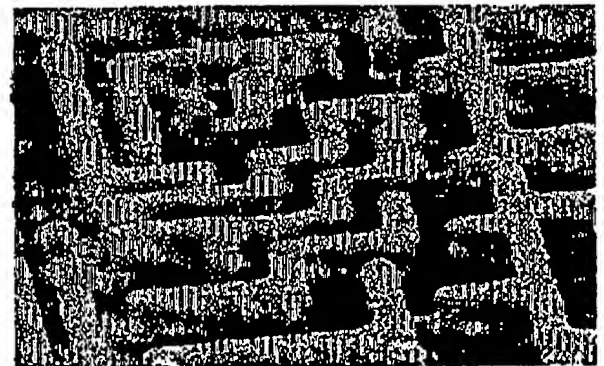


Fig. 4-41 A SEM of a Metal-1 interconnect-structure formed with W-plugs and Al:Cu interconnect-lines. Note that the ILD has been removed to make it possible to see the W-plugs. Photograph courtesy of ChipWorks.

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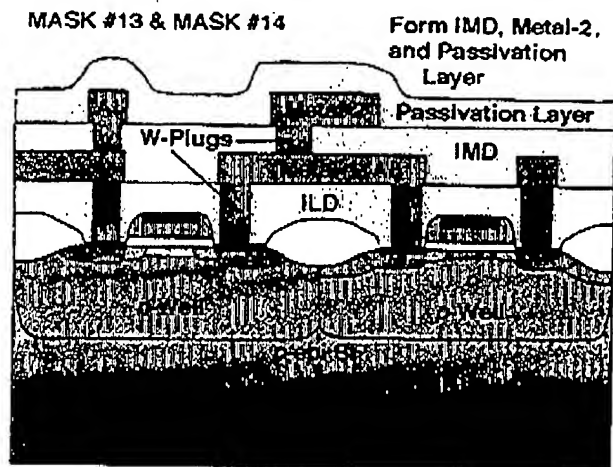


Fig. 4-42 Metal-2 is formed with the same steps as those shown in Figs. 4-35 to 4-40. *Mask #13* is used to define the via-holes between Metal-1 and Metal-2. *Mask #14* is used to define Metal-2. A final passivation-layer (typically CVD-oxide, or CVD-nitride - or both) covers the chip.

level-metal interconnect structure, but the faceplate of the chapter shows a cross-sectional drawing of an IC with 6-levels of metal.

To create the second interconnect-level, an *inter-metal dielectric (IMD)* must first be deposited. It electrically isolates the Metal-1 layer from the Metal-2 layer. Next, vias must be opened in this IMD-layer so that electrical connections can be established between Metal-2 and Metal-1 at desired locations (*Mask #13*).

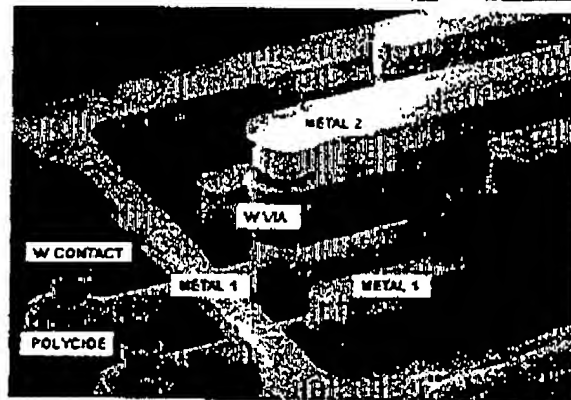


Fig. 4-43 SEM of an IBM circuit showing a two-level-metal interconnect structure formed with W-plugs and Al-lines. Photograph courtesy of Chip Works.

W-plugs and an Al:Cu-layer and a lithographic-step using *Mask #14* are used to form the Metal-2 interconnect-structures (Fig. 4-42). Figure 4-43 shows a SEM of a two-level-metal structure formed using Al-lines and W-plugs.

As noted above, more advanced ICs now use more than 2-levels of metal interconnects. Figure 4-44 shows a SEM of a four-level interconnect-structure. More details about fabricating such multilevel interconnect-structures are found in Chap. 24 and Ref. 3.

4.2.12 Passivation Layer and Pad Mask

Finally, a *passivation* (or *overcoat*) layer, such as CVD-PSG or plasma-enhanced-CVD silicon-nitride

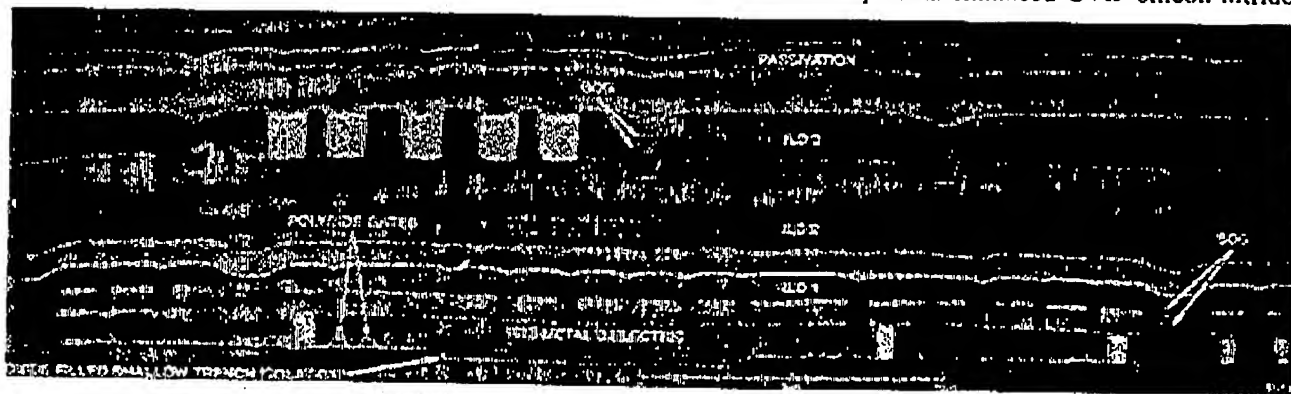


Fig. 4-44 SEM of 4-level-metal interconnect structure. Courtesy of ChipWorks.